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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/552,046	01/09/2007	Fung Leng Chen	Q74738	6904

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EXAMINER	
KUSUMAKAR, KAREN M	
ART UNIT	PAPER NUMBER
2829	

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02/26/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/552,046	CHEN ET AL.	
	Examiner	Art Unit	
	KAREN M. KUSUMAKAR	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-11 and 13-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2, 5-11 and 13-21* is/are rejected.

7)☒ Claim(s) *2 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. As of the amendment filed 2/11/09, no claims have been added, canceled, or amended. Therefore, claims 1, 2, and 5-21 remain pending, with claims 1, 10 and 17 being independent.

Response to Arguments

2. Applicant's arguments, see amendment filed 2/11/09, with respect to claims 1, 2, and 5-21 have been fully considered and are persuasive. The previous rejection has been withdrawn.

Claim Objections

3. Claim 1 is objected to because of the following informalities: "base" on line 12 should read –face--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 8, 10, 15, 16, 17 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Lee (US 2005/0040508)*** in view of ***Go et al. (US 2005/0012195).***

As to claims 1, 10 and 17, Lee teaches a ball grid array package comprising: a base IC structure (package 320b, Fig. 4), the base IC structure comprising: a base substrate (substrate 302 located on package 320b, packages 320b and 320a are almost identical and share the same numerals although not shown in the figures, Fig. 4) having a first base substrate face (top side of substrate 302 on package 320b that touches the chip 301 on package 320b, Fig. 4), a second base substrate face opposite to said first base substrate face (bottom side of substrate 302 on package 320b that touches external connection terminals 301, Fig. 4), a base substrate opening (opening 322 on package 320b, Fig. 4) extending between said first base substrate face and said second base substrate face, and a base conductor (wiring pattern 303 on package 320b, Fig. 4); a first semiconductor chip (Chip 301 on package 320b, Fig. 4), comprising a first chip face (top side of chip 301 on package 320b, Fig. 4), a second chip face opposite to said first chip face (bottom side of chip 301 on package 320b on which the bond pad is located, Fig. 4), and first bond pads disposed over said base substrate opening (located on bottom side of the chip in package 320b, Fig. 4); and a first plurality of wires (wires 304 of package 320b, Fig. 4) disposed to pass through said base substrate opening and electrically connecting said first bond pads to said base conductor (Fig. 4); and a secondary IC structure (package 320a, Fig. 4), comprising: a second substrate (substrate 302 on package 320a, Fig. 4) having a first secondary substrate face (top side of substrate 302 touching the chip 301 located on package 320a, Fig. 4), a second

secondary substrate face opposite to said first secondary substrate face (bottom side of substrate 302 touching the wiring pattern 303 located on package 320a, Fig. 4), a secondary opening (opening 322 in package 320a, Fig. 4) extending between said first secondary substrate face and said second secondary substrate face (p. 2, [0033], Fig. 4), and a secondary conductor (wiring pattern 303 located on package 320a, Fig. 4); a second semiconductor chip (chip 301 on package 320a, Fig. 4), comprising a first secondary chip face (top side of chip 301 located on package 320a, Fig. 4), and a second bond pad disposed over said secondary opening (located on bottom side of the chip in package 320a, Fig. 4); and a second plurality of wires (wires 304 located on package 320a, Fig. 4) electrically connecting said second bond pads to said secondary conductor through said secondary opening (p. 2, [0033], Fig. 4); and a third plurality of wires (flex cable with conductive patterns 306, Fig. 4) connecting said secondary IC structure to said base IC structure (p. 2, [0033], Fig. 4); wherein said secondary IC structure is mounted on said base IC structure (Fig. 4).

Lee is silent on a first encapsulant filling said secondary opening around said second plurality of wires and covering said second secondary substrate face. However, Go does teach a first encapsulant (protective member 140, p. 3, [0043], Fig. 12) filling said secondary opening around said second plurality of wires and covering said second secondary substrate face (protective member 140 at least partially covers the second substrate face, as shown in Fig. 12. In

the alternative, photo solder resist 116 combined with protective member 140 could be considered the encapsulant, which does completely cover both).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to encapsulate the wires and the substrate face so as to protect the wires and the interconnections of the package.

As to claim 8, Lee in view of Go further teaches at least one additional of said secondary IC structure mounted over said first secondary chip face (Lee, Fig. 7, third package from the bottom); and respective wires (Lee, flexible cable with conductive patterns 306, Fig. 7) connecting a conductive portion of said at least one additional secondary IC structure to said base IC structure (Lee, p. 3, [0035]).

As to claim 15, Lee in view of Go further teaches attaching solder balls (Lee, external connection terminals 307, Fig. 4) to the base IC structure (Fig. 4).

As to claim 16, Lee in view of Go further teaches singulation of the entire BGA structure (Lee, [0016], Lee refers to the structure as a single stack of packages, therefore it must have been singulated).

As to claim 21, Lee in view of Go further teaches the first IC chip and the second IC chip are substantially the same size (Lee, Fig. 4).

6. Claims 5-7, 11, 13-14 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Lee (US 2005/0040508)*** in view of ***Go et al. (US 2005/0012195)*** as applied to claims 1, 10 and 17, and in further view of ***Huang et al. (US 2002/0046854).***

As to claims 5-7, 13-14 and 18-20, Lee in view of Go teach all the limitations of claims 1, 10, and 17 but is silent on a molding compound encapsulating at least portions of said base IC structure and said secondary IC structure, wherein said molding compound encapsulates said third plurality of wires and said first secondary chip face is free of said molding compound.

However, Huang does teach encapsulating chips, including the wirings and the substrate (Fig. 1). Encapsulating a chip and its wirings in order to protect it is well known in the art and applying it to a plurality of stacked chips would not be a product of innovation but an art recognized solution for a common problem (i.e. protecting the chips).

Huang also teaches leaving a chip face free from the molding compound/encapsulant (p. 3, [0046], Fig. 8). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to leave a chip face free from the molding compound/encapsulant so as to allow heat to be released from the chip (Huang, p. 3, [0046]).

As to claim 11, Lee in view of Go and Huang further teaches first encapsulating said first secondary IC structure (Lee, encapsulant 305, Fig. 4). Lee in view of Go is silent on subsequently encapsulating said base IC structure and said first secondary IC structure, together with said first and second plurality of wires. However, Huang does teach encapsulating chips, including the wirings and the substrate (Fig. 1). Encapsulating a chip and its wirings in order to protect it is well known in the art and applying it to a plurality of stacked chips would not

be a product of innovation but an art recognized solution for a common problem (i.e. protecting the chips).

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over ***Lee (US 2005/0040508)*** in view of ***Go et al. (US 2005/0012195)*** as applied to claim 1, and in further view of ***Karnezos et al. (US 2004/0119152).***

As to claim 9, Lee in view of Go teach all the limitations of claim 1 but is silent on the package comprising a thermal dissipation element disposed over said first secondary chip face. However, Karnezos does teach a package comprising a thermal dissipation element (heat sink 530, Fig. 5D) disposed over a secondary chip face (die 514, Fig. 5D). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to add a thermal dissipation element to the package taught by Lee in view of Go so as to keep the chip from overheating.

Allowable Subject Matter

8. Claims 2 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art taken either singularly or in combination fails to anticipate or fairly suggest the limitations of the claims listed above in such a manner that a rejection under 35 U.S.C. 102 or 103 would be proper.

The prior art fails to teach a combination of all of the features in claim 2. In particular, the prior art fails to teach the base substrate further comprises a plurality of vias extending between said first base substrate face and said second base substrate face; said base conductor extends through said vias; and said base substrate further comprises a layer of solder mask disposed on portions of said first and second chip faces.

The prior art fails to teach a combination of all of the features in claim 12. In particular, the prior art fails to teach a third substrate and a third semiconductor chip mounted on said secondary substrate in a die-down configuration encapsulating said second secondary IC structure, such that encapsulant forms a substantially planar surface on the underside of said secondary IC structure; mounting the substantially planar surface of said encapsulant to said first secondary IC structure; electrically connecting a conductive portion of said second secondary IC structure to a conductive portion of at least one of said base IC structure and said first secondary IC structure; and connecting the second secondary IC structure to at least one of the base IC structure and the first secondary IC structure using a plurality of wires.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. ***Bai (US 2004/0061243)*** teaches a BGA package with wiring through a substrate aperture.

10. Any response to this Office Action should be faxed to (571) 273-8300 or mailed to:

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Hand-Delivered responses should be brought to:

Customer Service Window

Randolph Building

401 Dulany Street

Alexandria, VA 22313

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KAREN M. KUSUMAKAR whose telephone number is (571) 270-3520. The examiner can normally be reached on Mon - Thurs 7:30a - 5:00p EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/K. M. K./
Examiner, Art Unit 2829
2/20/2009

/Ha T. Nguyen/
Supervisory Patent Examiner, Art Unit 2829